Surface Morphology of Single and Multi-Layer Silicon Nitride Dielectric Nano-Coatings on Silicon Dioxide and Polycrystalline Silicon

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Silicon nitride (Si_3N_4) in a form of single and multi-layer nanofilms is proposed to be used as a dielectric layer in nanocapacitors for operation in harsh environmental conditions. Characterization of surface morphology, roughness and chemical bonds of the Si_3N_4 coatings has an important role in production process as the surface morphology affects the contact surface with other components of the produced device. Si_3N_4 was synthesized by using low pressure chemical vapour deposition method and depositing single and multi-layer (3 – 5 layers) nanofilms on SiO_2 and polycrystalline silicon (PolySi). The total thickness of the synthesized nanofilms was 20 – 60 nm. Surface morphology was investigated by means of scanning electron microscopy (SEM) and atomic force microscopy (AFM). Chemical bonds in the layers were identified by means of Fourier transform infrared spectrometry, attenuated total reflection (FTIR-ATR) method. (From the SEM and AFM images it was estimated that both single and multi-layer coatings are deposited homogenously. Si-N breathing and stretching modes are observed in FTIR spectra and the surface morphology is highly dependent on PolySi, therefore suggesting the decrease of the roughness of the bottom electrode for use in the nanocapacitors.
Keywords: silicon nitride, surface morphology, electron microscopy, atomic force microscopy.

1. INTRODUCTION

Silicon nitride (Si_3N_4) has a unique combination of electrical and mechanical properties: high dielectric constant, hardness and wear resistance, which are very advantageous under action of harsh conditions. It is proposed to use Si_3N_4 in space technology under action of ionizing radiation [1], for sensing applications [2], in Li-ion batteries and solar applications [3 – 8].

The capacitance of a capacitor increases when thickness of the dielectric decreases. However, the thickness of the dielectric in nanocapacitors is limited due to inhomogeneities arising at nanoscale. Defects that are present in the dielectric nanolayer will have a great impact on its performance. Therefore, the control of deposition technology for obtaining homogeneous and defect-free dielectric nanolayers is of great importance.

Si_3N_4 dielectric can be deposited as a single layer or as a multi-layer nanofilm. The main difference between the single layer and the multi-layer Si_3N_4 lies in the interfaces between the individual Si_3N_4 nano layers constituting the multi-layer film. The elemental composition at the interfaces differs from the bulk of the film, which can lead to changes in optical properties, breakdown voltage and leakage current characteristics of the multi-layer Si_3N_4 compared to the single layer film [9]. Content of oxygen can change at the interfaces between the individual Si_3N_4 nanolayers and this influences the formation of electrically active centres in the dielectric [10]. The multi-layer nanofilm is knows to have less pinholes compared to the single layer due to the fact that any pinholes present in an individual Si_3N_4 nanolayer will be covered by the next Si_3N_4 nanolayer during its deposition [9].

Characterization of surface morphology, roughness and chemical bonds of the Si_3N_4 coatings is required in order to estimate differences between single and multi-layer Si_3N_4 coatings. The surface morphology affects the contact surface with the other components of the produced device. By optimizing the synthesis conditions, it will be possible to improve the required properties according to the applications of the synthesized layers.

In this paper we investigate the chemical bonds and surface morphology of Si_3N_4 single and multi-layer coatings 20 – 60 nm thickness on SiO_2 and polycrystalline silicon (PolySi), in order to estimate differences between various synthesis parameters, two types of bottom electrode and to develop recommendations for producers.

2. EXPERIMENTAL DETAILS

The silicon nitride (Si_3N_4) layers were fabricated on the Si (76 mm) wafer (111 wafer surface). The wafer was oxidized at 1130 °C in the oxygen environment for 2 hours. The thickness of SiO_2 was 1 μm. Polycrystalline Si layer (PolySi) was deposited on SiO_2 as a bottom electrode of the nanocapacitor. The deposition of PolySi was performed in

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the atmosphere of SiH_4 and N_2 gases at 900 °C during 40 minutes. The thickness of PolySi was 0.4 µm. Deposition of the conductive polycrystalline Si layer was done in SiH_4 and N_2 gases atmosphere during 40 minutes at 900 °C, the layer was doped with phosphorus (gases: $POCl_3$, $O_2 + N_2$; 15 minutes; 900 °C); a thickness of the layer was 0.4 µm. Si_3N_4 dielectric nanolayer was deposited on the PolySi electrode using Low Pressure Chemical Vapour Deposition (LPCVD). Si_3N_4 was synthesized performing a reaction: $SiH_4 + NH_3$ at 800 °C, achieving the single or multi-layer coating. The multi-layer coating consisted of several Si_3N_4 nanolayers. To fabricate Si_3N_4 multi-layer, the inflow of SiH_4 was stopped after the deposition of the first Si_3N_4 nanolayer, and its surface was annealed in a NH_3 stream at 800 °C for 10 minutes. After the annealing, deposition of the next Si_3N_4 nanolayer was performed. The process of the deposition and annealing was repeated several times to obtain desired number of Si_3N_4 nanolayers. Several types of the Si_3N_4 coatings were synthesized: 20 and 25 nm single (assigned as 1×) and 3 layered (3×) coatings, 40 and 60 nm single (1×) and 5 layered (5×) coatings.

The surface morphology of single and multi-layer coatings was measured by SEM (field emission scanning electron microscope Hitachi S-4800) and AFM (Asylum Research MFP-3D atomic force microscope). AFM imaging was performed in tapping mode using NT-MDT NSG10 probes. The roughness parameters *R*a and *R*q were calculated from AFM images with a scan size 3 × 3 µm and 256 × 256 data points using Igor Pro software according to Eq. 1 and Eq. 2:

$$Ra = \frac{1}{N}\sum_{i=1}^{N}|Z_i - \bar{Z}|; \quad (1)$$

$$Rq = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(Z_i - \bar{Z})^2}, \quad (2)$$

where Z_i is the height at a given pixel i, N is the total number of pixels in the image, $\bar{Z}$ is the average height of the entire image.

The Fourier transform infrared (FTIR) spectra were recorded with Bruker Vertex 70v spectrometer - equipped with an attenuated total reflection (ATR) module that contains a diamond crystal with refractive index 2.4. The spectra were recorded in a spectral range of 4000 – 400 cm^{-1}, in vacuum 2.95 hPa, resolution ± 2 cm^{-1}, 20 scans per measurement.

3. RESULTS AND DISCUSSION

3.1. Characterisation of surface chemical bonds

The 20 – 60 nm single and multi-layer Si_3N_4 coatings were analysed with means of infrared spectrometry, attenuated total reflection. The samples were analysed prior and after deposition of each layer. The silicon substrate gives a signal around 510 cm^{-1}. By depositing SiO_2, the Si signal does not occur in the spectrum and intensive signals of Si-O streching, bending and rocking occur [3]. By covering the SiO_2 the PolySi layer doped with phosphorous, Si-O bonds, the intensity of Si-O bonds significantly decreases. In the spectrum of the Si_3N_4 single and multi-layer coatings on the PolySi the main bonds occur in the range of 400 – 1300 cm^{-1}.

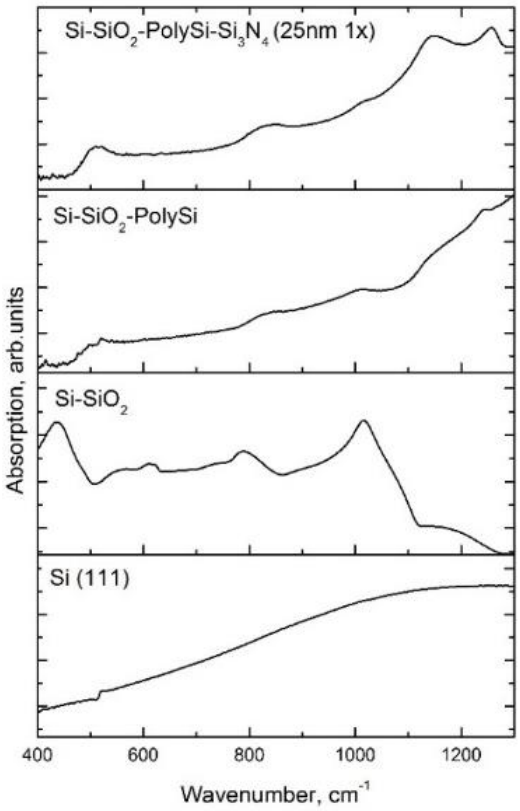

Fig. 1. FTIR spectra of (from bottom to top) Si substrate, Si coated with SiO_2, Si coated with SiO_2 and PolySi doped with P, Si coated with SiO_2, PolySi doped with P and coated with single layer Si_3N_4

The FTIR spectra of the each deposited coating are presented in Fig. 1.

In Fig. 1, where Si_3N_4 coating is deposited, a signal around 490 – 530 cm^{-1} could be due to Si-N breathing [11] and Si-N stretching mode [12].

The signal at 840 cm^{-1} is due do Si-N bonds [13], while at 1000 – 1100 cm^{-1} the signals occur due to Si-N stretching [7, 13] and presence of Si-O-N [11].

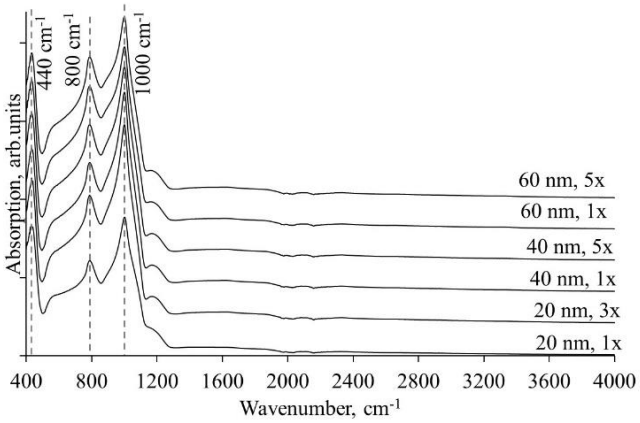

Fig. 2. FTIR spectra of deposited Si_3N_4 single and multi-layer coatings on the Si substrate covered with SiO_2

FTIR spectra of the Si_3N_4 coatings on the surface of SiO_2 are presented in Fig. 2. The multiplication sign in the description of the spectrum shows the number of individual Si_3N_4 nanolayers in the particular coating. In the spectra

strong signals of the Si-O bonds are timed. The Si-N bonds are not clearly visible. To determine the influence of the synthesis method and the number of Si-N layers on the chemical composition of the surface, the FTIR spectra of the Si_3N_4 coatings were analysed. The main signals occur in the range of $900 - 1200\ cm^{-1}$ and they are due Si-N bonds. Spectral distortions that occur in the range of $1900 - 2300\ cm^{-1}$ [15] are probably due to the similar values of refractive indices of the diamond crystal and the synthesized Si_3N_4. The FTIR spectra of the Si_3N_4 coatings on the PolySi are presented in Fig. 3. In the FTIR spectra the Si-N signal intensities are similar in both cases, single and multi-layer Si_3N_4 coatings.

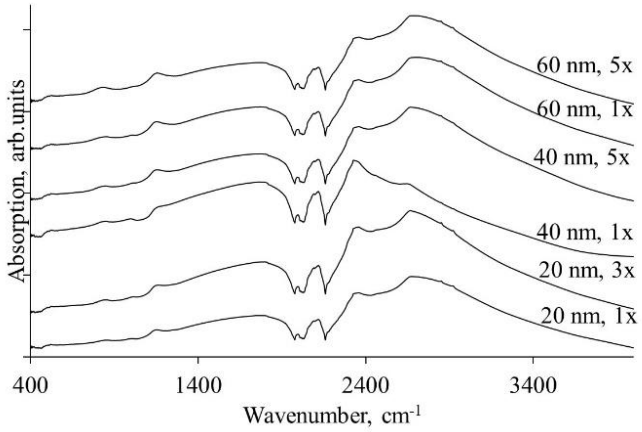

Fig. 3. FTIR spectra of deposited layers on the Si substrate covered with SiO_2 and PolySi doped with P

To compare the morphology of the single and multi-layer Si_3N_4 coatings, SEM and AFM measurements were performed. AFM image of PolySi deposited on SiO_2 shows that the PolySi has a relatively rough surface (Fig. 4).

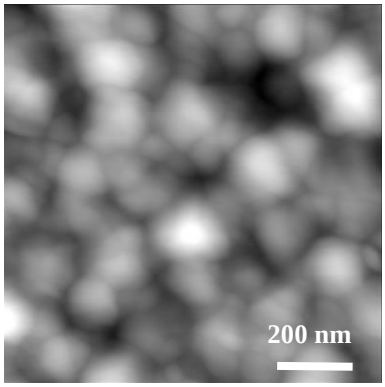

Fig. 4. AFM image of a PolySi on the Si covered with SiO_2

SEM images of the single and multi-layer Si_3N_4 coatings deposited on PolySi are shown Fig. 5a and Fig. 5b respectively. The fine grains of Si_3N_4 homogeneously and fully cover the bigger bumps formed by PolySi, no pinholes to the PolySi surface were observed. The size of Si_3N_4 grains obtained from the SEM measurements is in the range of $15 - 40$ nm for both the single layer and multi-layer coatings.

SEM and AFM measurements demonstrated that the total thickness of Si_3N_4 dielectric and number of individual Si_3N_4 nanolayers do not influence surface morphology of Si_3N_4. However, the surface morphology is determined by the underlying layer. Height profiles of SiO_2, PolySi layers and Si_3N_4 layers deposited either on PolySi or SiO_2 were extracted from AFM images (Fig. 6).

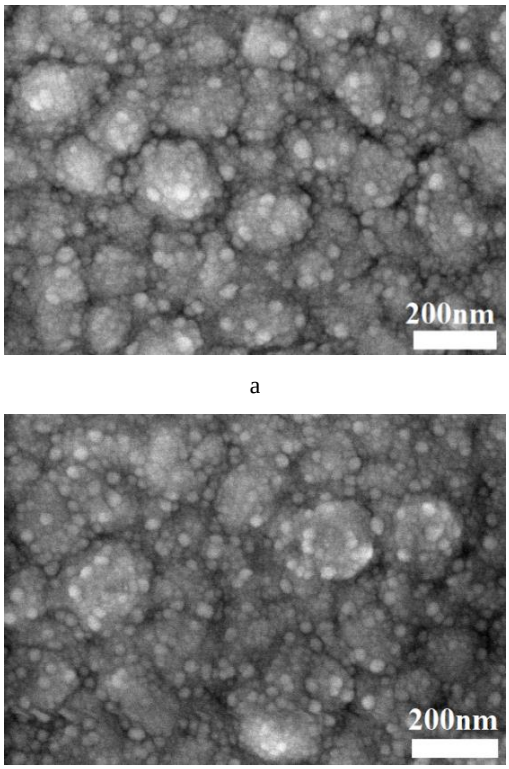

Fig. 5. SEM image of a 40 nm thick Si_3N_4 nanolayer deposited on PolySi: a – single layer; b – multi-layer

The height profiles of PolySi and Si_3N_4 deposited on PolySi are similar, having bumps with heights around $10 - 20$ nm. The height profile of Si_3N_4 deposited on a relatively smooth SiO_2 shows little bumps with heights in the range of $1 - 3$ nm. Fig. 7 shows the roughness parameters *R*a and *R*q measured for each layer of the Si-SiO_2-PolySi-Si_3N_4 structure. In the case of SiO_2 as the underlying layer with *R*a = 151 pm (*R*q = 201 pm), *R*a of Si_3N_4 is 1.2 ± 0.1 nm (*R*q = 1.4 ± 0.1 nm). In the case of PolySi as the underlying layer with *R*a = 8.7 nm (*R*q = 11.0 nm), *R*a of Si_3N_4 is 8.5 ± 0.3 nm (*R*q = 10.5 ± 0.4 nm).

The morphology measurements demonstrated that when PolySi is used as a bottom electrode of a nanocapacitor, the surface morphology of Si_3N_4 dielectric is determined by PolySi. In this case the roughness of Si_3N_4 is comparable with the total thickness of the dielectric. This is undesirable for nanocapacitors, since it causes dielectric breakdowns at high voltages and increases leakage currents due to the local amplification of the electric field at surface peaks and changes in the local thickness of the dielectric between two adjacent electrodes [15]. This means that controlling the roughness of the bottom electrode plays a critical role in nanocapacitors. The roughness of the bottom electrode should be minimized either by selecting the appropriate electrode material or by adjusting the deposition technology.

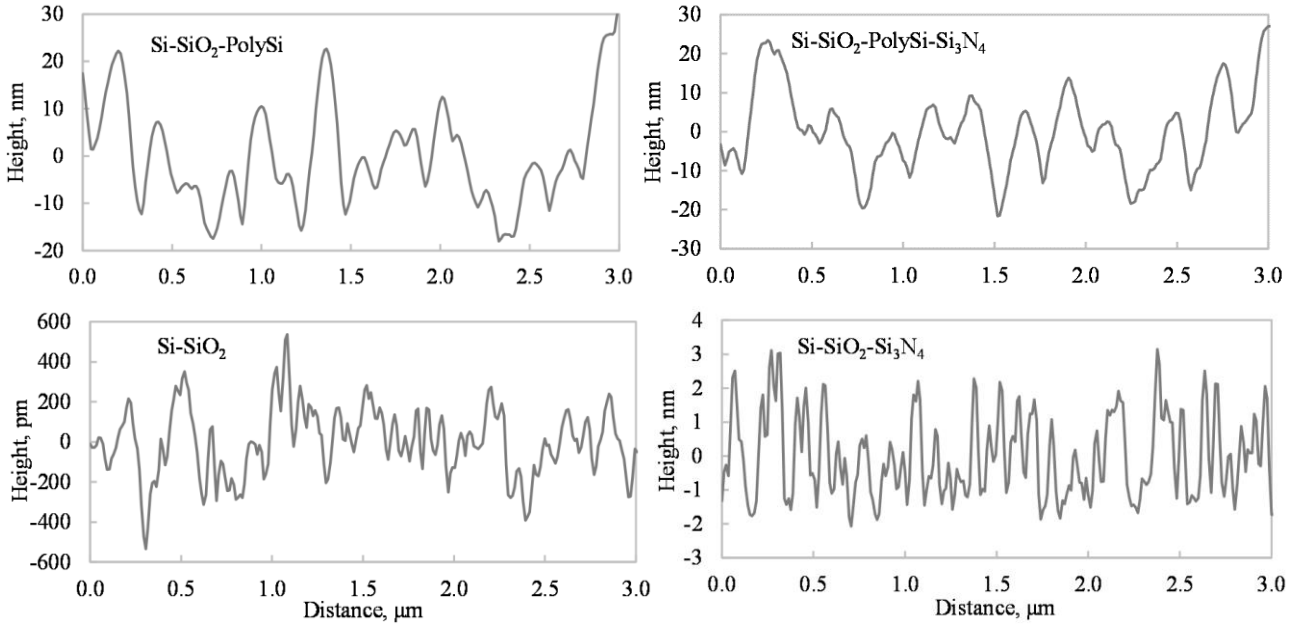

Fig. 6. Height profiles of SiO_2, PolySi layer and Si_3N_4 nanolayer deposited either on PolySi or SiO_2

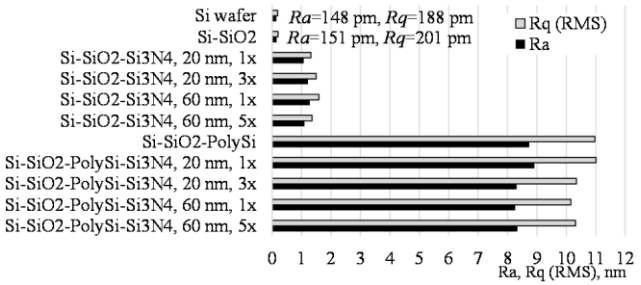

Fig. 7. Roughness parameters *Ra* and *Rq* of Si wafer, SiO_2, PolySi layers and Si_3N_4 nanolayers deposited either on PolySi or SiO_2 layer

4. CONCLUSIONS

Si-N breathing and stretching modes are observed in the FTIR spectra of deposited layers, however in the case, where Si_3N_4 is deposited on the top of SiO_2, the SiO_2 bonds are dominant.

The surface roughness and morphology of 20 – 60 nm thick single and multi-layer Si_3N_4 coatings deposited by LPCVD are similar. The sizes of Si_3N_4 grains are in the range of 15 – 40 nm. The coatings are deposited homogenously over the underlying layer and no pinholes to the underlying layer are observed.

In the case of a nano thick Si_3N_4 dielectric, its surface morphology and roughness is highly dependent on the roughness of the underlying layer. Therefore, the choice of the appropriate material of the bottom electrode for use in nanocapacitors is very important. The roughness of the bottom electrode has to be less or similar to the roughness of Si_3N_4. The roughness of PolySi as the bottom electrode was comparable to the thickness of Si_3N_4, which is undesirable as it increases the probability of dielectric breakdown at high voltages and increases leakage currents. The roughness of the bottom electrode should be minimized either by selecting the appropriate electrode material or by adjusting the deposition technology.

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