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# Epitaxial Growth and Properties of Silicon on Crystalline Rare-Earth-Metal Oxide for SOI-Applications

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Silicon on isolator technology decreases effects of parasitic capacitance and leakage between the circuit components that limit the density of transistors in the conventional bulk complementary metal oxide semiconductor field effect transistor technology. There are several methods for fabrication of SOI substrates. Additional fabrication costs for SOI substrates limit application of this technology for production of main stream chips. New technological solutions and materials are needed. Two new approaches for fabrication of silicon on isolator structure with crystalline gadolinium oxide as buried oxide are studied. The first approach is based on the formation of a template single crystalline Si-layer and combines encapsulated solid-phase epitaxy of silicon on rare-earth-metal-oxide layer (developed for fabrication of oxide/silicon/oxide heterostructures), subsequent chemical etching of the second oxide layer, followed by vapor-phase epitaxial growth of silicon on the template-silicon layer. In the second method, crystalline single oriented silicon islands serve as seed for further epitaxial growth of a crystalline Si layer on gadolinium oxide. Structural investigations show that the overgrown silicon layer is structurally coherent with the template silicon layer with no distinguishable difference at the interface. Silicon-substrate/oxide/silicon heterostructure exhibits transition of the substrate crystalline structure with A/B/A twinning relationship and in A/B/B relationship in some regions. The initial stage of deposition of the template silicon is crucial for its structural quality.
*Keywords:* silicon on isolator, MBE, rare earth metal oxide, high-k dielectrics.

## INTRODUCTION

Exponential scaling of integrated circuits (IC) governed by Moore's Law leads to additional effects (parasitic capacitance, increased leakage current, short channel effect, latch-up) that limit performance enhancement and increase power consumption of bulk-Si electronic devices pushing them to a number of fundamental limits. The implementation of silicon on isolator (SOI) technology is one of the possible solutions that allow further miniaturization of IC and increasing of its performance. The isolator layer can effectively reduce short channel effects, eliminate parasitic capacitance and most of the leakage paths. Application of SOI-technology enhances performance by up to 30 percent and reduces power consumption between 30 and 60 percent if compared to similar bulk-technology chips with the same clock speed [1 – 3]. It is worth noting that this improvement in performance roughly corresponds to the performance gain obtained by jumping ahead one technology generation of conventional bulk-Si ICs. Additionally, SOI-technology based devices show high radiation and thermal hardness – properties important for devices used for space technology. In the methods used for fabrication of SOI substrates, usually $SiO_2$ acts as isolating layer. However, the active semiconductor layer on top has to be single crystalline with high perfection. Separation by an amorphous $SiO_2$ makes technology more complicated, thus, the cost of SOI-technology-based devices are approximately 10 % higher than that of bulk technology [4]. The main drawback of SOI on wafer scale is the low thermal conductivity of $SiO_2$ leading to a significant temperature increase within the active device area. This limits application of SOI technology. Another approach is to employ the buried isolation only locally. Using such technique in a BiCMOS technology, CMOS devices could be fabricated on SOI regions, while bipolar transistors were fabricated on bulk regions with good crystalline structure. However, such local SOI structures can only be produced by separation by implantation of oxygen (SIMOX) leading to strong structural degradation in the top Si layer.

Here, we will present methods for the epitaxial growth of a crystalline isolator followed by the fabrication of the crystalline Si layer. The application of an epitaxially grown crystalline isolator as buried oxide (BOX), should make fabrication of SOI structures less complicated and less expensive.

Recently, epitaxial rare-earth-metal-oxide (REMO) layers have already proved to be a potential candidate for future high-K dielectric in ultra-scaled complementary metal oxide semiconductor field effect transistor applications [5]. This material also offers the opportunity to realize buried isolator structures by epitaxial growth of single crystalline Si directly on crystalline isolator layers. The fabrication of an epitaxial Si/isolator/Si heterostructure requires not only the growth of atomically flat and defect-free isolating barriers on a Si substrate, but also the growth of an epitaxial Si layer on the isolator. The latter cannot be achieved straightforwardly because of the differences in surface free energy between the isolator and silicon. Unconventional growth methods have to be found to solve

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this problem. Based on different investigations [6, 7], we developed two approaches for the fabrication of heteroepitaxial stacks with buried crystalline rare-earth-metal-oxide.

The first approach is based on encapsulated solid-phase epitaxy (SPE), in which the crystallization of amorphous silicon is accompanied by vapor-phase epitaxy of a second isolator layer. The second approach combines SPE of crystalline silicon islands that serve as template, followed by vapor-phase epitaxial growth of a silicon layer.

In the present work, we will demonstrate the potential of both methods for fabrication of silicon-on-rare-earth-metal-oxide structures.

## EXPERIMENTAL

The crystalline heterostructures were grown on Si(111) substrates using a multi-chamber molecular beam epitaxy (MBE) system (DCA Instruments). The substrates were HF cleaned and immediately introduced into the MBE system. After this treatment, the substrates exhibited the hydrogen-terminated (1×1) surface structure. Silicon and commercially available, granular stoichiometric $Gd_2O_3$ material were evaporated by electron beam evaporation with typical rates of 0.01 nm/s – 0.03 nm/s. The evaporation rate of silicon was controlled by a mass-spectrometer. Additional molecular oxygen was supplied into the chamber using a piezo-leak-valve during the growth of gadolinium oxide to avoid silicide formation [8]. The partial pressure of oxygen in the chamber was kept constant at $5\times10^{-7}$ mbar. The formed structures were investigated *in situ* by reflection high-energy electron diffraction (RHEED) and *ex situ* by X-ray diffraction (XRD) and transmission electron microscopy (TEM). The thickness of the formed layers was measured *ex situ* using X-ray reflection (XRR).

## RESULTS AND DISCUSSION

The first approach for the epitaxial growth of silicon layer on crystalline gadolinium oxide is based on the method for fabrication of oxide/silicon/oxide heterostructures for quantum-well devices (Fig. 1).

First, an epitaxial $Gd_2O_3$ layer was grown on a (111) oriented silicon substrate. No additional *in situ* surface preparation was applied. The growth was started at 650 °C. The streaky-like RHEED patterns with three additional substreaks appeared during the growth, as shown in Fig. 2. This indicates a very well oriented, layer by layer grown gadolinium oxide layer with a very flat surface.

As it was discussed in detail in our earlier experiments [6, 7], silicon does not wet the gadolinium oxide surface under common epitaxial conditions. Therefore, modified growth is necessary to realize smooth epitaxial Si-layers. Si was deposited at 90 °C to prevent island formation kinetically. The gradual transition from a two-dimensional (2D) to a diffuse RHEED pattern (not shown here) observed during the growth indicates the formation of an amorphous Si layer. After that, the temperature was increased (200 °C/min) up to 650 °C to realize SPE of silicon. In order to suppress Si surface migration and to avoid formation of islands the Si layer must be encapsulated by $Gd_2O_3$ before crystallization of Si starts. The growth of $Gd_2O_3$ was started already at 200 °C, since $Gd_2O_3$ tends to grow in (111) orientation even on amorphous layer [9]. The growth sequence of the encapsulated solid phase epitaxy is shown in the Fig. 3. At the temperature of about 400 °C, a streaky RHEED pattern appears similar to that of the first $Gd_2O_3$ layer (shown in Fig. 2) indicating growth of a crystalline gadolinium oxide layer. The final thickness of the upper $Gd_2O_3$ layer is 2 nm – 3 nm. The deposition rate of $Gd_2O_3$ has a significant influence on the structure of the silicon layer.

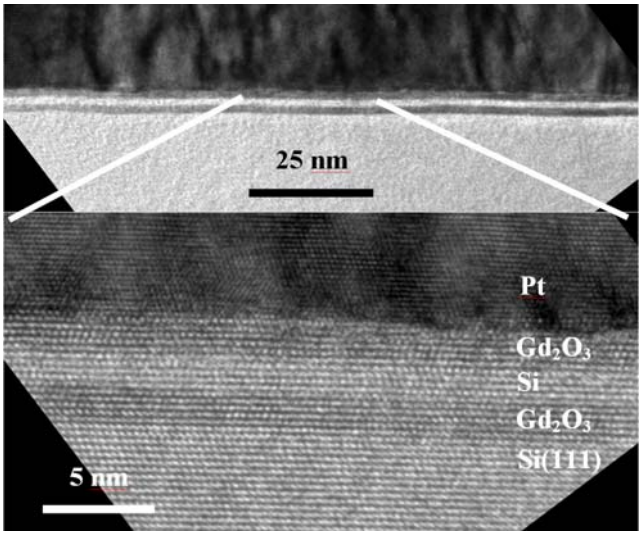
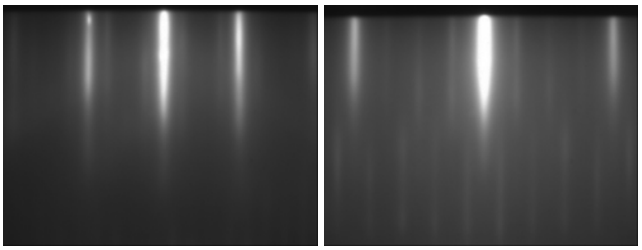



**Fig. 1.** HRTEM micrographs of $Gd_2O_3$/Si/ $Gd_2O_3$ double barier structure grown on Si(111) by solid-phase-epitaxy [7]



a b

**Fig. 2.** Typical RHEED patterns of 4 nm $Gd_2O_3$ grown on Si(111) obtained in (a) ⟨110⟩ and (b) ⟨112⟩ azimuth

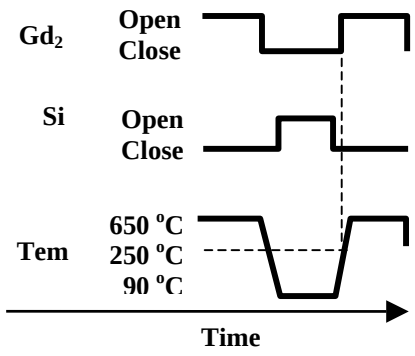



**Fig. 3.** Sequence of source supply and substrate temperature during encapsulated solid phase epitaxy

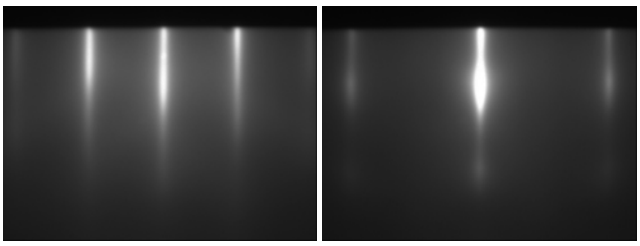


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**Fig. 4.** RHEED patterns of SPE grown template Si layer obtained in (a) ⟨110⟩ and (b) ⟨112⟩ azimuth after wet-chemical etching of the upper $Gd_2O_3$ layer

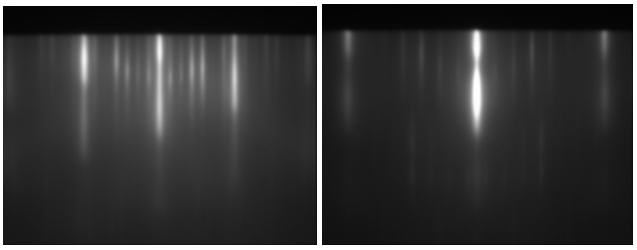

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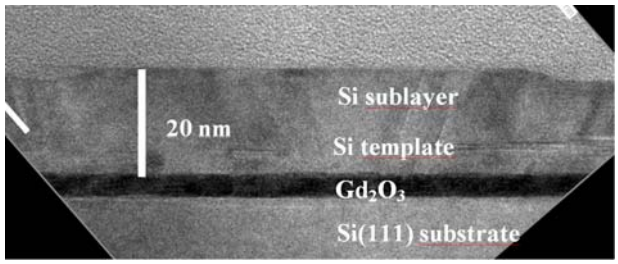
**Fig. 5.** RHEED patterns of a Si film grown on a template Si layer in (a) ⟨110⟩ and (b) ⟨112⟩ azimuth

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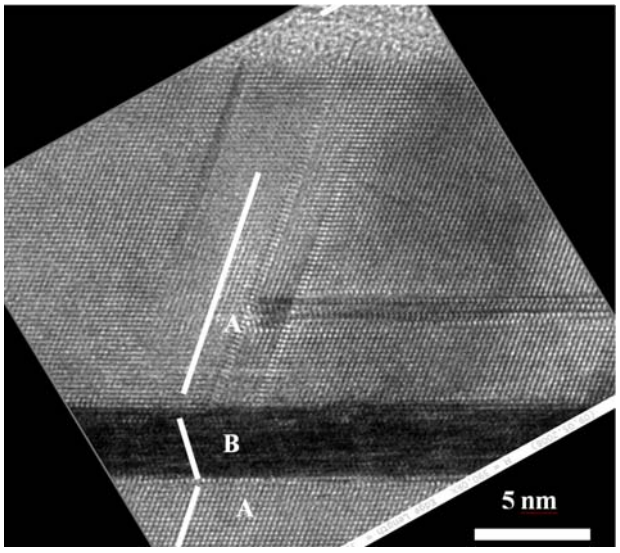


b

**Fig. 6.** Cross-sectional low (a) and high (b) magnification TEM micrographs of Si (111)/$Gd_2O_3$/Si structure. Si was epitaxially grown on a template layer

If the rate is too low, the Si layer is not completely encapsulated before crystallization occurs, leading to Si clusters partially coated with $Gd_2O_3$. In the case of high $Gd_2O_3$ deposition rate, a polycrystalline Si layer will be formed. As it was shown earlier [6], the first crystalline $Gd_2O_3$ layer acts as the seed for crystallization of the amorphous Si layer. The crystallization front moves from the lower to the upper Si/$Gd_2O_3$ interface. After $Gd_2O_3$ growth, the temperature was immediately ramped down to room temperature.

Then, the upper $Gd_2O_3$ layer was removed by wet-chemical etching in 1 % $H_2SO_4$ solution. Because of the high selectivity the etching stops at the Si layer, leading to a crystalline template for further Si growth. Subsequently, diluted HF was used to remove any formed silicon oxide. After etching, the sample was immediately re-loaded into the MBE system. The chemically processed sample exhibits a clean (1×1) surface structure, indicating SPE growth of encapsulates Si on $Gd_2O_3$ (Fig. 4). That is supported by the appearance of the 7×7 reconstruction of the clean well ordered Si(111) surface during thermal preparation in a slight Si-flux at 700 °C temperature (not shown here). After that preparation, the temperature was ramped down to 300 °C for further growth of silicon. The Si growth was started at 300 °C with moderate growth rate of approximately 0.005 nm/s to enable the formation of a well ordered transition between the template and the growing film. Subsequently, the growth temperature was increased with 10 °C/min up to 600 °C. Simultaneously, the Si growth rate was also increased gradually to approximately 0.015 nm/s. During and after the growth, RHEED patterns exhibit 7×7 reconstructed surfaces, as shown in Fig. 5, indicating good epitaxial growth of the silicon layer on the template. The final structure is shown in Fig. 6. It exhibits an A/B/A orientation relationship between Si substrate, gadolinium oxide, and Si layer. Here, the Si(111) substrate and Si layer are in A orientation, and the oxide layer is rotated by 180° around the [111] axis with respect to Si corresponding to the B orientation. This is confirmed by an XRD Phi-scan (Fig. 7), which also shows the 180° rotation of $Gd_2O_3$ with respect to Si. The Si(111)/$Gd_2O_3$/Si interfaces are very abrupt with no obvious traces of amorphous $SiO_2$. The structure shows good crystalline quality indicating possible application of this procedure for growing SOI structures. However, some defects occur in the silicon layer. These defects are

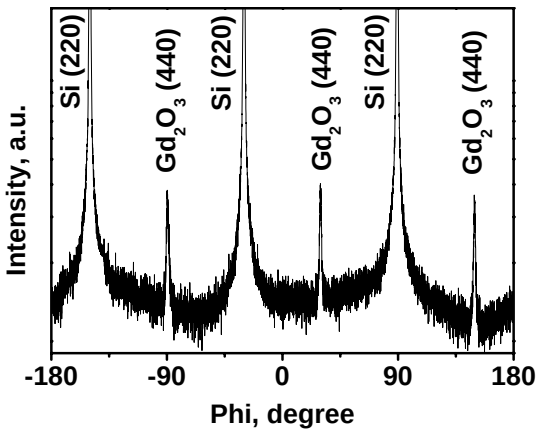


**Fig. 7.** Phi-scan of Si (111)/$Gd_2O_3$/Si structure

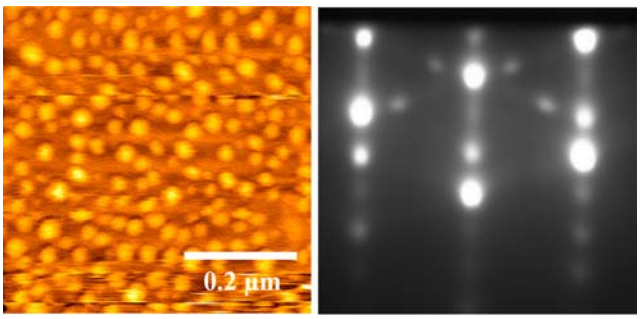


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**Fig. 8.** AFM picture (a) and RHEED pattern (b) of Si islands grown on $Gd_2O_3$ [10]

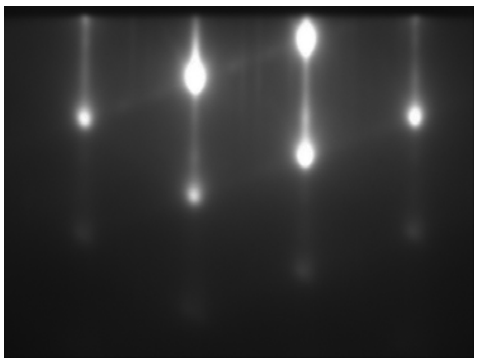
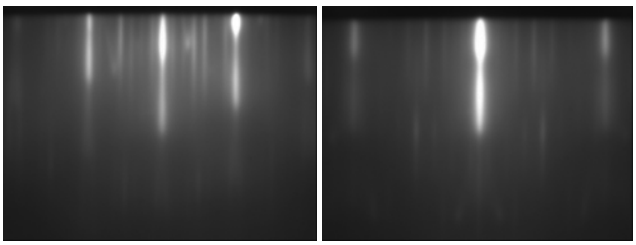


**Fig. 9.** RHEED pattern in ⟨110⟩ azimuth of single oriented Si islands formed by SPE



a b

**Fig. 10.** RHEED patterns of a single oriented Si layer formed on Si islands (in (a) ⟨110⟩ and (b) ⟨112⟩ azimuth)

inclined twinning lamellae correlated to surface steps of the oxide layer. Furthermore, stacking faults occur in the growth direction of the Si layer. This kind of defect is caused likely by Si nucleation on contaminated surface regions, remaining after wet-chemical etching.

Next, we discuss the possibility to grow a crystalline Si-layer on Si islands in order to avoid the growth of the capping $Gd_2O_3$ layer and, finally, to simplify the total growth procedure. It is known, that formation of twinned (A- and B-oriented) Si-islands on rare earth metal oxides is energetically favorable in conventional epitaxial growth (Fig. 8, a). Double spots in the RHEED pattern indicate formation of twinned islands as shown in Fig. 8, b. Subsequent growth of Si on such twinned islands would lead to the formation of twins in the layer. To prevent this severe problem, Si islands have to be single oriented. Based on recent investigations [7, 10], SPE was used to obtain single oriented islands. First, a very thin (thickness 2 nm – 3 nm) amorphous Si layer was deposited on single crystalline gadolinium oxide layer at 90 °C by gradual increase of growth rate. The growth was stopped after a

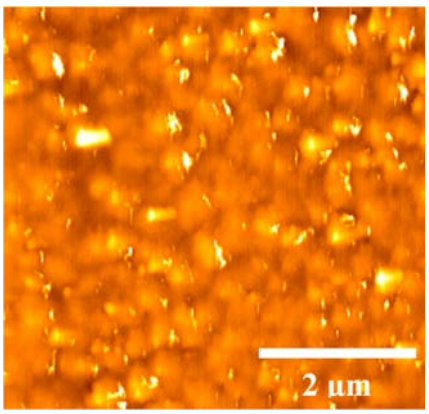
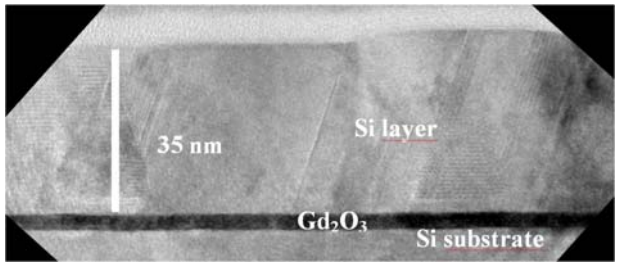



**Fig. 11.** AFM picture of a Si layer grown on single oriented Si islands

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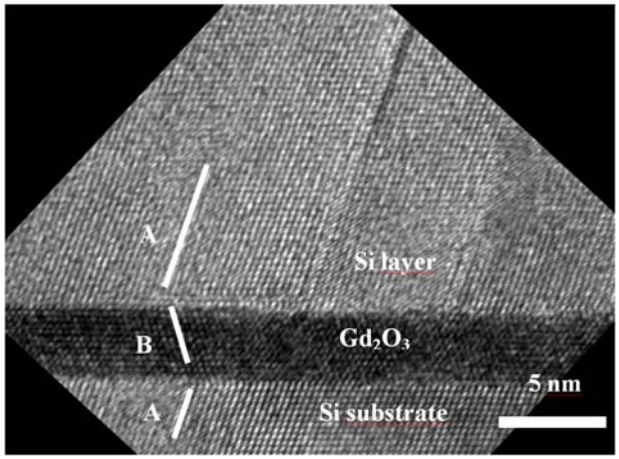


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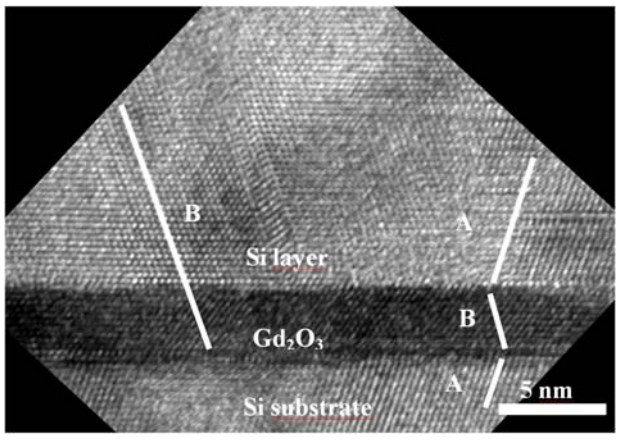


c

**Fig. 12.** Cross-sectional low (a) and high (b), (c) magnification TEM micrographs of Si (111)/$Gd_2O_3$/Si structure. The Si layer was grown by vapour phase epitaxy on single oriented crystalline Si islands

transition from 2D to diffuse RHEED pattern occurred. Subsequently, the temperature was ramped to 650 °C with a rate of 200 °C/min in order to form crystalline Si islands.At about 400 °C, a 3D RHEED pattern appears, indicating the formation Si islands. The orientation of those islands was found to dependent critically on the deposition rate of the amorphous layer. Only in case of low (0.005 nm/s) rate, single oriented islands could be obtained. In this case no double spots were found in the RHEED pattern (Fig. 9). This indicates that very small silicon nanocrystallites in perfect orientation are already formed by deposition of Si at 90 °C. These crystallites act as seeds for subsequent crystallization of Si islands at higher temperatures. Subsequent growth of a Si layer on the single oriented islands was started at 300 °C to overgrow the islands without roughening of the surface. Then, the temperature was ramped to 600 °C with a rate of 200 °C/min in order to get further flattening of the Si layer. During the growth, a gradual transition from 3D to 2D RHEED pattern was observed (Fig. 10), what indicates overgrowth of Si islands and flattening of the Si surface. The roughness of the surface was evaluated by atomic force microscopy. AFM pictures of the layer show overgrown islands (Fig. 11), the surface of the Si layer is still rough. The root mean square roughness of the surface is 2.5 nm. TEM micrographs (Fig. 12) show that the formed Si layer consists of A and B oriented regions, although single oriented Si islands serve as crystallization seeds for the MBE-grown layer. Most likely, the B oriented regions in the Si layer are formed during the MBE of Si at temperatures above 300 °C on the free oxide surface between the Si-islands. Usually, Si islands in twin orientation to each other, that means in A and B orientation, were formed during conventional Si MBE on rare-earth metal oxides [10]. The main defects are twin lamellae correlated with surface steps. There are also large defect-free regions.

## CONCLUSIONS

Growth of silicon on crystalline gadolinium oxide based on solid phase epitaxy was studied. The formed ultra thin crystalline Si layer or single oriented crystalline Si islands act as a template for vapor phase epitaxy of Si. The studied approaches can be considered as promising methods for the epitaxial growth of silicon on isolator structures. It could be suitable for production of SOI wafers in less expensive and less complicated way or for application of locally buried isolators.

Further study will be appointed for optimization of the silicon growth parameters and gadolinium oxide wet chemical etching procedure.

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