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A New Vertical p-GaN Island Double-Trench MOSFET with High Voltage Resistance and Low Leakage

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Due to the higher breakdown voltage (V_{DSmax}) and anticipated improved reliability, vertical gallium nitride (GaN) metal-oxide-semiconductor field-effect transistors (MOSFETs) are a focal point in next-generation power device research. This paper, based on DC characteristic simulations of various trench-structured GaN MOSFETs, proposes a novel p-GaN island double-trench MOSFET (P-Island DT-MOS) device. Compared to single-trench MOS devices with identical structural parameters, the double-trench structure of this device achieves a lower peak electric field in the oxide layer. Furthermore, the incorporation of the p-GaN island enhances V_{DSmax} to 1.74 kV. Due to the reduced gate-drain charge in the P-Island DT-MOS, its high-frequency figure of merit (HF-FOM) is 47 % lower than that of the DT-MOS. The findings of this study are significant for achieving high breakdown voltage and low on-resistance in vertical GaN double-trench MOS devices.
Keywords: vertical GaN, double-trench, breakdown voltage, p-GaN island.

1. INTRODUCTION

Since the turn of the 21st century, integrated circuit systems have continuously evolved toward smaller sizes, higher power densities, and higher operating frequencies. GaN materials, with their wide bandgap, high breakdown electric field, high electron mobility in heterojunctions, and high 2DEG concentration, as well as a Baliga figure of merit (BFOM) superior to that of silicon carbide (SiC) and silicon (Si), are considered among the most promising materials for power electronics applications [1]. Currently, 650V lateral GaN High Electron Mobility Transistors (HEMTs) have been commercialized. Compared to GaN HEMTs, vertical GaN devices offer several potential advantages: (1) higher breakdown voltage and power density; (2) reduced electric field crowding near the device surface, leading to greater reliability; and (3) better thermal management, extending device lifetime [2]. These benefits position vertical GaN devices as particularly advantageous for high-voltage applications exceeding 1.2 kV, such as in train and ship transportation, power transmission grids, electric vehicles, solar inverters, industrial power supplies, and other similar fields [3].

In high-voltage environments, the performance of GaN power devices largely hinges on advancements in GaN single-crystal materials and the development of vertical GaN power device technology [4]. Several kilovolt-level GaN vertical transistors have been reported in the literature, including the Current Aperture Vertical Electron Transistor (CAVET) [5], vertical trench MOSFET [6], vertical trench MOSFET based on in-situ oxidized GaN layers (OG-FET) [7], and vertical GaN FinFETs [8]. Among the common vertical GaN MOSFETs, trench-type MOSFETs are capable of achieving higher positive threshold voltages and utilize P-type body layers and lightly doped drift regions to form PN junctions, thereby achieving high breakdown voltage. However, the trench bottom region of vertical GaN trench MOSFETs is prone to electric field concentration, leading to premature breakdown with a breakdown voltage far below the theoretical value of GaN PN junctions. Therefore, suppressing the electric field at the trench corner under off-state conditions is critical for enhancing the device's breakdown voltage. Several solutions have been proposed, including thick bottom dielectric (TBD) [9], double gate dielectric layers (Al_2O_3 and SiO_2) [10], vertical field plate oxide [11], and P-type implanted junction termination [12], all of which have successfully reduced the electric field at the trench corner region. However, most of the existing research remains at the simulation stage [13], with significant challenges related to process complexity, and the breakdown voltage has not been substantially enhanced. The maximum breakdown voltage of a vertical GaN channel MOSFET is primarily determined by the avalanche breakdown mechanism. In this context, reference [14] demonstrates an increase in breakdown voltage to 1602 V through a careful optimization of the P-type doping concentration.

To enhance the breakdown voltage and figure of merit (BFOM) of vertical GaN trench MOSFETs while achieving an optimal balance between high breakdown voltage and low on-resistance, this paper employs TCAD software to perform a comprehensive parameter optimization for vertical GaN double-trench MOSFET (DT-MOS) devices. The study highlights the potential advantages of the double-channel design. Furthermore, a novel DT-MOS structure featuring a p-GaN island positioned beneath the gate groove

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is proposed. In order to characterize the off-state breakdown voltage of MOS devices, the maximum voltage is set as the blocking voltage where the electric field strength at any point of the grid dielectric reaches 3 MV/cm. Simulation results indicate that, compared to the structure reported in [15], the proposed DT-MOS structure elevates the off-state breakdown voltage from 1.5 kV to the 1.7 kV level, achieving a final Baliga's figure of merit (BFOM) of 1.34 GW/cm^2. This study marks the first effort to measure the gate charge of vertical GaN double-trench MOSFET devices. It has been observed that while the double-trench structure mitigates the adverse effects of p-implantation on the device's conduction characteristics and enhances the breakdown voltage, it also introduces a non-negligible gate leakage current. The proposed vertical GaN DT-MOS with a p-GaN island not only significantly reduces gate leakage but also demonstrates lower switching losses than anticipated.

2. DEVICE STRUCTURE OPTIMIZATION DESIGN

Fig. 1 illustrates the half-cell cross-sectional view of the vertical GaN DT-MOS device, arranged from top to bottom as follows: etched gate and source regions, n$^+$ source region, p-base channel region, p$^+$ source region, n$^-$ drift layer, and n$^+$ substrate. The half-cell width of the device structure is 2.8 μm, with both sidewall and bottom oxide thicknesses of 0.05 μm. The n- drift layer has a thickness of 11 μm and a doping concentration of 5×10^{15} cm^{-3}, while the substrate thickness is 1 μm. Detailed device structure parameters are provided in Table 1. This paper mainly uses the SDevice module of Sentaurus TCAD to simulate the electrical properties of trench MOSFETs. The area factor is set to 1000, and the following simulation models are used: the basic carrier generation and recombination model (Shockley-Read-Hall) SRH and (Auger) recombination, high doping-induced incomplete ionization, high-field carrier velocity saturation, and the doping-dependent mobility model and avalanche breakdown model. In the avalanche breakdown model, the carrier generation rate can be expressed as:

$$G = \alpha_n n u_n + \alpha_p p u_p, \tag{1}$$

where $\alpha_{n,p}$ is the impact ionization rate; n and p are the concentrations of electrons and holes, respectively. van Overstraeten-de Man model [16] has been adopted in this simulation, which is based on the Chynoweth model [17]:

$$\alpha(E) = \gamma a exp(-\frac{\gamma b}{E}), \tag{2}$$

where:

$$\gamma = \frac{tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)}. \tag{3}$$

In GaN material, the values of a are 1.1438×10^7 cm^{-1} and 1.34×10^8 cm^{-1}, corresponding to the values of electrons and holes respectively, and the values of b are 4.7786×10^7 and 2.0300×10^7 respectively. $\hbar\omega_{op}$ is 0.035 eV.

Heavily doped p^+ source region and low-doped n^- drift layer in vertical GaN DT-MOS device structure form PN junction, following the expression of avalanche breakdown voltage when PN junction is reversely biased [18]:

$$V_B = \frac{1}{2}\left(\frac{\varepsilon_0\varepsilon_s}{q}\right)^{3/4}\left(\frac{8}{C_i}\right)^{1/4}\left(\frac{N_A N_D}{N_A+N_D}\right)^{-3/4}, \tag{4}$$

where C_i is a constant related to the effective ionization rate; N_A and N_D are acceptor concentrations in the p^+ source region and donor concentrations in the n^- drift layer, respectively.

Table 1. Summary of key parameters

Parameter	DT-MOS
Gate trench depth, t_{gate}	1.5 μm
Gate trench width, w_{gate}	2 μm
Thickness of gate dielectric, t_{ox}	50 nm
Source trench width, w_{source}	varied
Source trench depth, t_{source}	1.5 μm
n$^+$-source layer thickness, t_{nsoure}	0.2 μm
n$^+$-source layer doping concentration, N_{nsoure}	5×10^{18} cm^3
p-channel region thickness, $t_{channel}$	0.5 μm
p-channel region doping concentration, $N_{channel}$	2×10^{17}/cm^3
p$^+$ region thichness, t_{p^+}	varied
p$^+$ region doping concentration, N_{p+}	1×10^{18}/cm^3
Drift layer thickness, t_{drift}	11 μm
Drift layer doping concentration, N_{drift}	5×10^{15}/cm^3

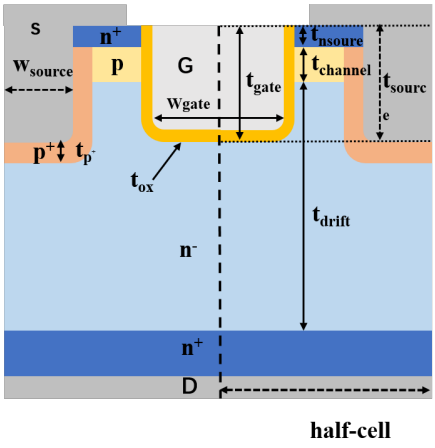


Fig. 1. Structure cross-section of DT-MOS device

For vertical GaN double-trench MOSFETs, the thickness of the p^+ source region (t_{p^+}) and the width of the source trench (w_{source}) are two critical structural parameters in the field-shielding design. These parameters have a significant impact on both the breakdown characteristics and conduction performance of the device.

To simplify the analysis, we take the DT-MOS with a source trench width of 1 μm as an example, designing t_{p^+} to vary between 0.2 μm and 0.8 μm. As shown in Fig. 2, as t_{p^+} gradually increases, the breakdown voltage of the device in the off-state decreases continuously. Fig. 2 also illustrates the variation in the maximum electric field in the gate oxide layer when the drain voltage (V_{DS}) is 1200 V in the off-state. As the p^+ source region thickness increases, the maximum electric field at the bottom corner of the gate oxide layer decreases accordingly. With the increase of the thickness of the p$^+$ source region, the number of immovable negative charges provided by the p$^+$ source region in the depleted state gradually increases, and the thickness of the effective drift region is further thinned, which together leads to the

continuous weakening of the breakdown characteristics of the device.

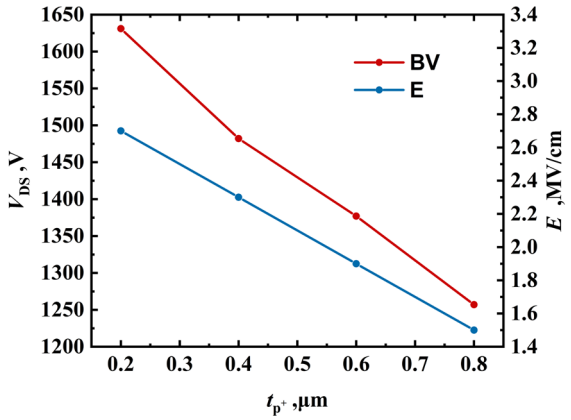


Fig. 2. The effect of t_{p^+} change from 0.2 μm to 0.8 μm on the breakdown characteristics of the device

Fig. 3 shows that the increased thickness of the p^+ source region enhances the depletion ability of the drift region at the gate trench corner, thus reducing the electric field intensity at the gate trench corner. The transfer and output characteristics were showed in Fig. 4, that the drain current density I_{DS} gradually decreases as t_{p^+} increases, and the result indicated a negative impact of the increased p^+ source region thickness on the device's on-state performance. The current path is affected by the p^+ source region, and the effective drift region area also gradually decreases.

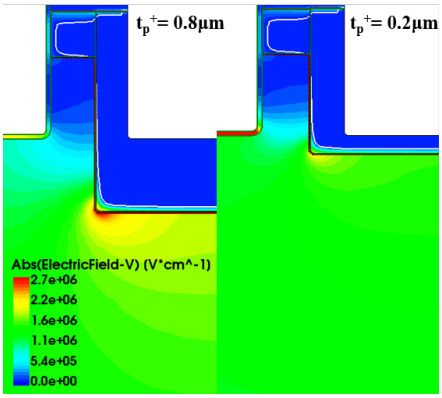


Fig. 3. The change of electric field strength when t_{p+} changes from 0.2 μm to 0.8 μm

Taking the optimized structure (t_{p^+} = 0.2 μm) as an example, three devices with source trench widths of 0.8 μm, 1 μm, and 1.2 μm were simulated. As shown in Fig. 5, the off-state breakdown voltage of the device increases progressively with the widening of w_{source}. Furthermore, under a drain voltage of 1200 V in the off-state, the maximum electric field at the bottom corner of the gate oxide layer decreases from 3.1 MV/cm to 1.9 MV/cm. As the source trench width increases, the distance between the two p^+ source regions gradually decreases, which is related to the weakening of the electric field near the bottom of the gate oxide layer in the drift region. With an increase in the source trench width, the immobile positive charge in the drift region near the bottom of the gate dielectric layer decreases, thus reducing the need for excessive negative charge from the p-base and p^+ source regions.

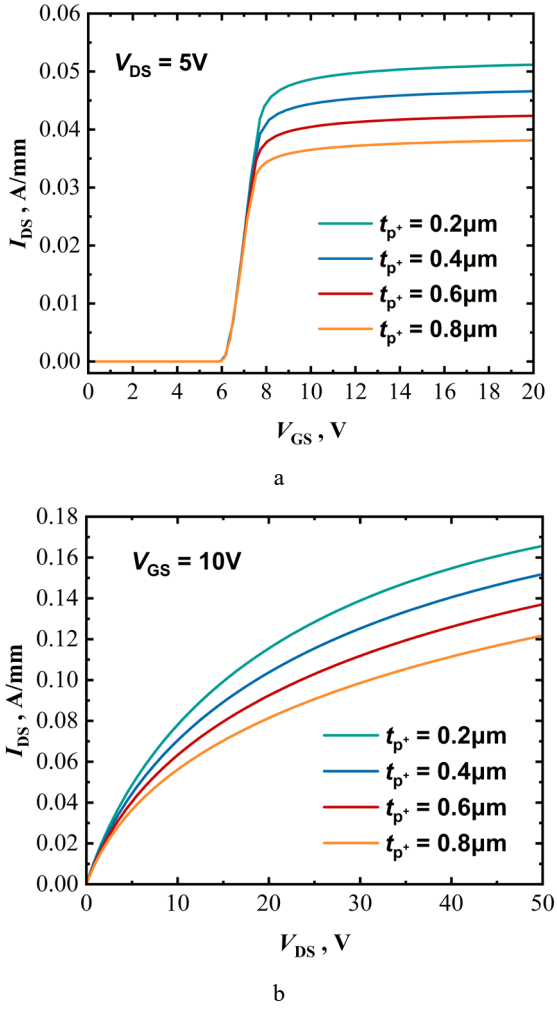


Fig. 4. Characteristics at different t_{p^+}: a – transfer; b – output

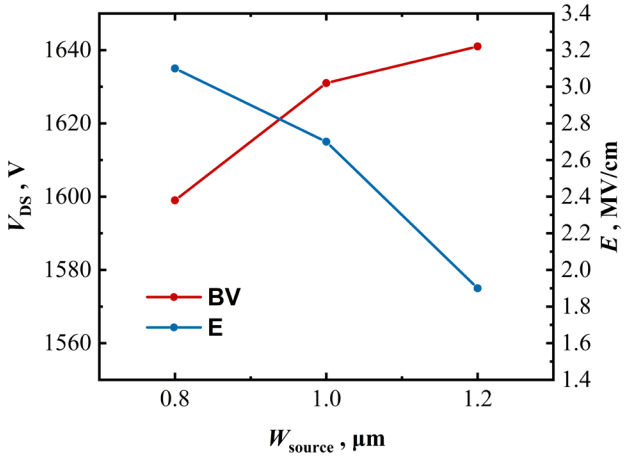


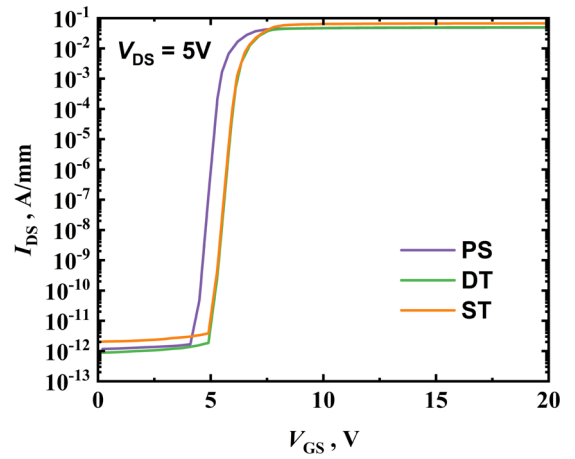
Fig. 5. The effect of w_{source} change from 0.8 μm to 1.2 μm on the breakdown characteristics of the device

As a result, the corner near the interface between the p^+ source region and the n^- drift region can sustain a higher electric field, thereby improving the breakdown voltage of the device. Ultimately, we select the device with w_{source} = 1.2 μm and t_{p^+} = 0.2 μm as the final optimized configuration.

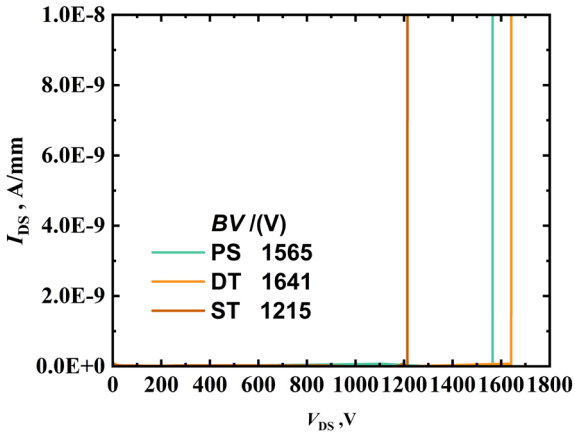
2. RESULTS AND ANALYSIS

2.1. Comparison of electrical characteristics of vertical GaN trench MOSFET

Based on the parameter-optimized vertical DT-MOS, this paper compares its electrical characteristics with those of single-trench ST-MOS and p^+-field-shielded PS-MOS devices. Fig. 6 a, b, and c respectively illustrate the transfer characteristics, output characteristics, and breakdown characteristics of the three device types.



a



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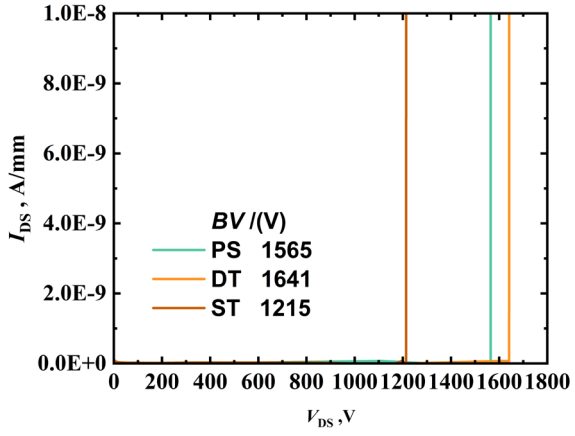
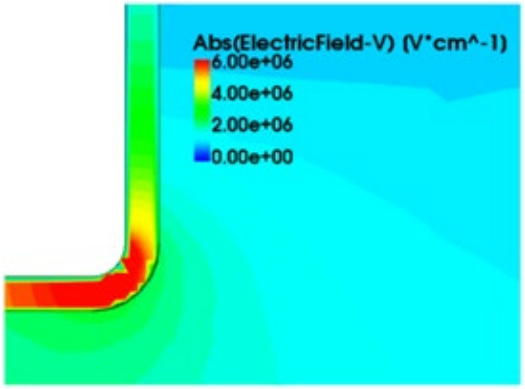


c

Fig. 6. Comparison of transfer characteristics, output characteristics and breakdown characteristics of ST-MOS, DTMOS and PS-MOS

From the transfer characteristic curves, the threshold voltages of the DT-MOS, ST-MOS, and PS-MOS are extracted as 5.9 V, 5.9 V, and 5.3 V, respectively. Compared with the PS-MOS, the DT-MOS maintains relatively stable threshold voltage characteristics. When the drain voltage equals 10 V, the DT-MOS exhibits the highest on/off ratio, approximately 10^{11}. As shown in the output curves in Fig. 6 b, at V_{DS} = 50 V, the saturation drain current I_{Dsat} for the ST-MOS reaches 194 mA/mm, surpassing that of both the DT-MOS and PS-MOS (I_{Dsat} = 166 mA/mm, I_{Dsat} = 155 mA/mm, respectively). The on-resistance extracted from the linear region of the output curve for ST-MOS, DT-MOS, and PS-MOS is 66 mΩ, 69 mΩ, and 88 mΩ respectively. Fig. 7 a, b, and c display the electric field distribution at the bottom corner of the gate oxide layer under an off-state drain voltage of 1200 V for the three types of devices.



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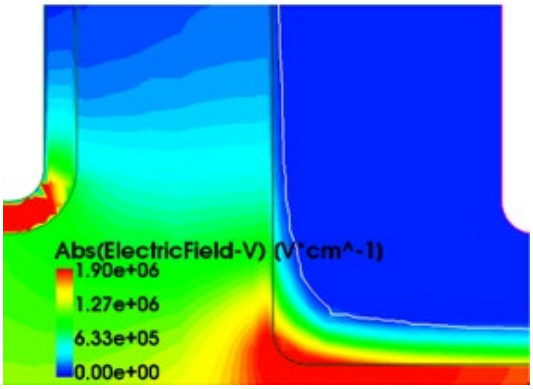

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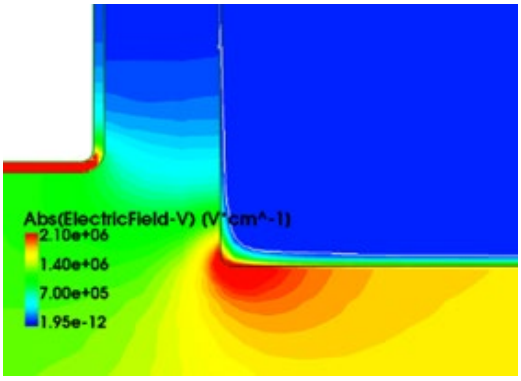


c

Fig. 7. Absolute values of electric field strength at V_{GS} = 0 V and V_{DS} = 1200 V for: a – ST-MOS; b – DT-MOS; c – PS-MOS

Based on the simulation results, the electric field intensity at the corners of the gate oxide layer in ST-MOS devices reaches up to 6 MV/cm, significantly exceeding the reliability threshold for 50 nm thick silicon dioxide (SiO_2) used as the gate dielectric [19]. Both alternative gate structures significantly mitigate the electric field concentration at the bottom corner of the gate oxide layer, with the maximum electric field intensity of DT-MOS being lower than that of PS-MOS. The p^+ source region, as a field shielding structure, reduces the electric field applied to the gate oxide layer, ensuring that the peak electric field in the gate oxide layer of PS and DT MOSFETs is below 3 MV/cm. The results indicate that the combined effect of the source trench and p^+ region prevents premature breakdown of the gate oxide layer, transferring the internal electric field of the gate trench bottom oxide layer to the reverse-biased PN junction depletion region, thus alleviating the electric field concentration in the gate oxide layer. However, this negatively impacts the on-state performance of the devices, though the source-trench structure of the DT-MOS is beneficial for improving the device's conduction characteristics. The above conclusions are consistent with those obtained in literature [15]. It is worth noting that this work reduces the peak electric field of oxygen corner of the trench gate with the same thickness from 2.3 MV/cm to 1.9 MV/cm by means of reasonable device structure optimization, while increasing the maximum operating voltage to 1600 V. The calculated specific on-resistance is 1.93 mΩ•cm^2, which is slightly lower than the on-resistance in literature [16]. It also proves that the device structure optimization method is of great significance to achieve high breakdown voltage and low on-resistance.

2.2. New vertical p-GaN island double-channel MOSFETs

Based on the simulation analysis framework presented above, this paper proposes a novel DT-MOS structure, as shown in Fig. 8.

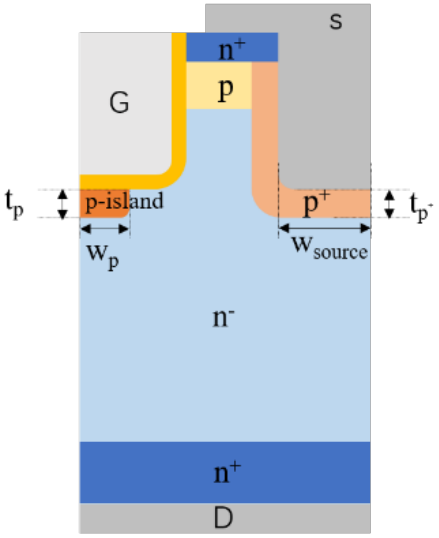


Fig. 8. Cross-section of DT-MOS half cell structure with p-GaN island

In this optimized DT-MOS, a p-GaN island is inserted directly beneath the gate. The key parameters for optimizing the device include the thickness (t_p), width (w_p), and doping concentration (N_p) of the p-GaN island. Through optimization (t_p = 0.25 μm, w_p = 0.5 μm, N_p = 3 × 10^{17}/cm^3), as illustrated in Fig. 9, the device achieved a breakdown voltage in the off-state of 1744 V. From the transfer and output characteristic curves, the current on/off ratio of the P-island DT-MOS is extracted as 10^{11} (V_{DS} = 10 V), with a threshold voltage shift of 5.9 V. When V_{DS} = 50 V, the saturation drain current I_{Dsat} = 122 mA/mm, and the device's on-resistance is 81 mΩ (Fig. 10).

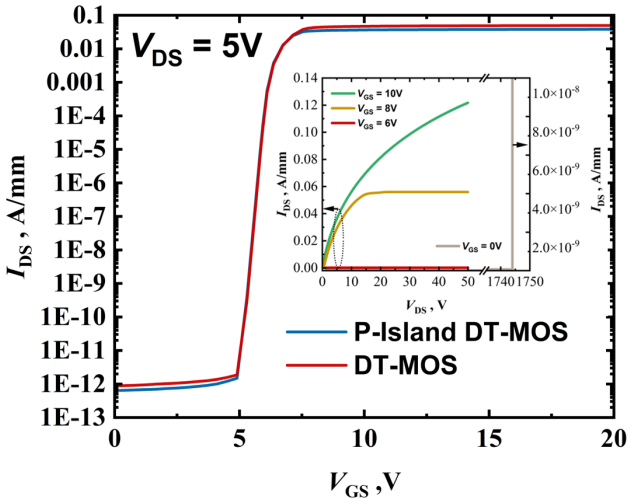


Fig. 9. I – V characteristics of p-island DT-MOS and DT-MOS in forward and blocked states

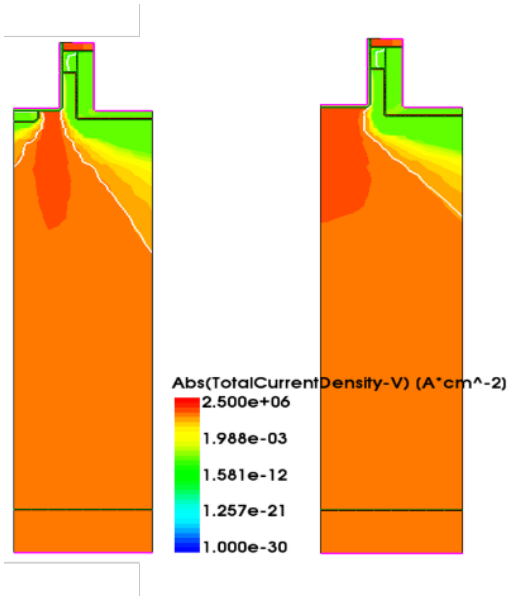
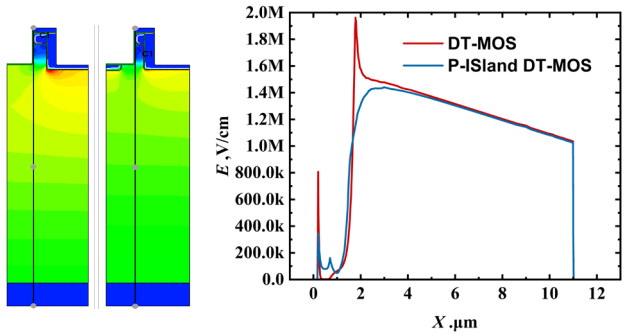


Fig. 10. Current density distribution of p-island DT-MOS and DT-MOS at V_{GS} = 10 V and V_{DS} = 50 V

Compared to the optimized DT-MOS, the DT-MOS with the p-GaN island shows an increase in off-state breakdown voltage from 1641 V to 1744 V, with a slight reduction in forward conduction characteristics. As shown in Fig. 11, the current density distribution of the two DT-MOS structures at V_{GS} = 10V and V_{DS} = 50V is presented. Due to the insertion of the p-GaN island, the current path in the new DT-MOS becomes significantly narrower, as the adjacent regions of the p-GaN island are depleted, reducing the effective drift region area. This design effectively

enhances the off-state breakdown voltage of the device. At this time, the maximum breakdown voltage of the device is no longer determined by the maximum electric field at the corner of the trench, but is dominated by the avalanche breakdown mechanism [19].



a b

Fig. 11. p-island DT-MOS and DT-MOS at 1200 V: a – electric field intensity distribution; b – absolute value of electric field intensity along the cutting line through the gate oxide layer

Fig. 11 a shows the electric field distribution at an off-state of 1200 V for both the new DT-MOS with the p-GaN island and the optimized DT-MOS. It can be observed that the insertion of the p-GaN island significantly improves the maximum electric field distribution in the PN junction depletion layer formed between the p^+ source region and the *n*- drift layer, while also mitigating the electric field concentration at the p^+ source region corners. The curve in Fig. 11 b illustrates the absolute value of the electric field strength along the cutline shown in Fig. 11 a. The results indicate that the presence of the p-GaN island reduces the peak electric field at the bottom of the gate oxide layer from the previous 1.9 MV to 1.3 MV, greatly reducing the electric field applied to the gate oxide layer. The reason is that the depletion region formed by the p-GaN island in the drift region overlaps with the depletion region of the p^+ source in the same area. This combined depletion effect extends the electric field in the transverse direction under the gate, thereby reducing the electric field intensity within the gate's oxide layer. Consequently, the off-state voltage resistance of the device is no longer constrained by the gate oxide layer but is instead determined by the avalanche breakdown of the PN junction. This characteristic is highly advantageous for enhancing the reliability of GaN power devices [20]. Ultimately, the BFOM of the p-island DT-MOS is determined to be 1.34 GW/cm², which is higher than the maximum BFOM obtained in literature [14]. Through rational parameter optimization, the power characteristics of the conventional trench MOSFET have been significantly enhanced.

Fig. 12 presents the gate leakage current curves for the ST-MOS, DT-MOS, and p-island DT-MOS devices, where both the source voltage (V_S) and the drain voltage (V_D) are set to 0 V during gate leakage measurements. As shown, the gate leakage current in the double-trench structure is slightly higher than that in the single-trench structure. However, the double-trench structure with a p-GaN island does not exhibit a significant increase in gate leakage current, indicating that the insertion of the p-GaN island effectively suppresses gate leakage. This suppression effect is attributed to the complete depletion of the region beneath the gate by the p-GaN island, which reduces the concentration of charge carriers injected into the gate. This result suggests that the p-island DT-MOS has the potential to enhance gate voltage withstand capability.

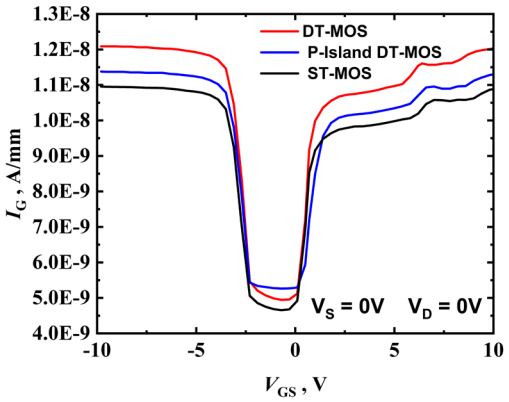
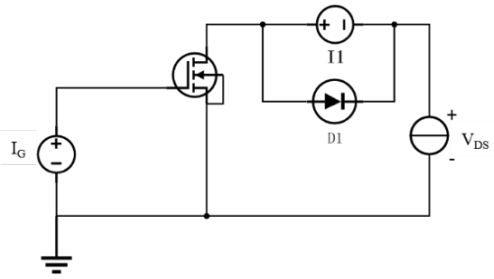


Fig. 12. Gate leakage curves of ST-MOS, DT-MOS and p-island DT-MOS

Based on the previous simulation results, the vertical GaN DT-MOS device demonstrates the optimal current switching ratio, approximately 10^{11}, indicating that the dual-trench structure MOSFET offers superior switching performance. In the switching loss of power MOSFETs, the gate-drain charge (Q_{GD}) is a critical parameter [21]. Fig. 13 a illustrates the test circuit for the gate charge, and Fig. 13 b shows the simulated gate charge waveforms for the newly designed p-island DT-MOS and the optimized DT-MOS at V_{DS} = 30 V, I_D = 5 A, and I_G = 0.1 mA.



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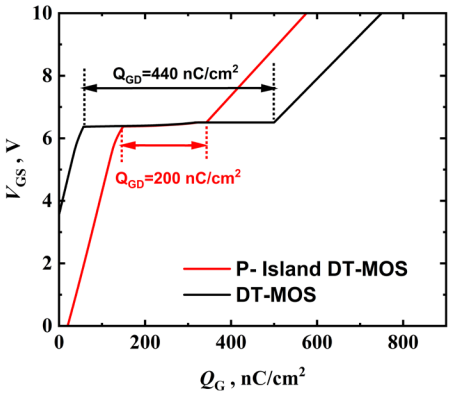

b

Fig. 13. a – gate charge test circuit; b – comparison of gate charge waveforms of p-island DT-MOS and DT-MOS

After optimization, the Q_{GD} of the DT-MOS featuring a p-GaN island amounts to 440 nC, while that of the DT-MOS without a p-GaN island is 200 nC, indicating that the p-GaN island directly below the gate converts part of the gate-to-drain capacitor C_{GD} into leak-to-source capacitor C_{DS}, thus significantly reducing the gate leakage charge Q_{GD}. The comparison of the calculated high-frequency superiority factor (HF-FOM ($Q_{GD} \times R_{ON}$)) reveals that the value of the p-island DT-MOS is 460 nC • mΩ, which is approximately 47 % lower than that of the DT-MOS lacking a p-GaN island (867 nC • mΩ), suggesting that the p-island DT-MOS with a p-GaN island has lower switching losses.

A potential device fabrication process is proposed, as illustrated in Fig.14, which consists of the following steps: First, light-doped N-type GaN drift regions are grown by metal-organic chemical vapor deposition (MOCVD) on a GaN self-supporting substrate. Next, a SiO_2 mask is applied, followed by the selective epitaxial growth of P-type GaN using MOCVD.

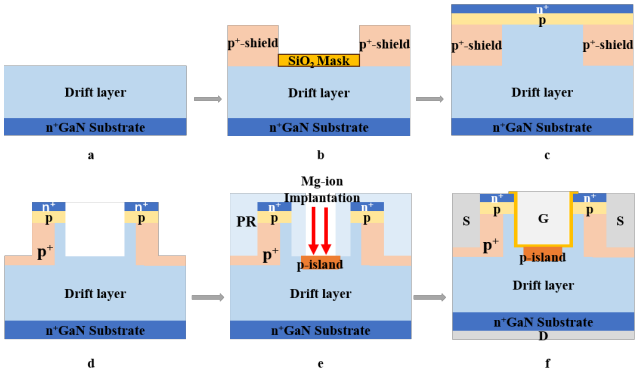

Fig. 14. Potential process manufacturing flow for p-island DT-MOS including MOCVD selection epitaxy and ion implantation

The SiO_2 mask is then removed by etching by reactive ion etching (RIE) method Subsequently, the GaN drift layer is filled via MOCVD epitaxy, followed by horizontal epitaxy. The p-base channel region and n^+ source region, typical of conventional structures, are then grown using MOCVD. Inductively coupled plasma (ICP) etching is employed to create gate and source grooves, exposing the buried p^+ source region. Photoresist is used as an ion implantation mask, and a p-GaN island is formed through selective P-type doping via Mg ion implantation [22]. The epitaxial wafer is then placed in the MOCVD reaction chamber to activate the buried p-type GaN. SiO_2 gate dielectric is deposited by plasma enhanced chemical vapor deposition (PECVD), and finally, the source, gate, and drain contacts are fabricated by magnetron sputtering, with Ni/Au used for the gate and Ti/Al/Ni/Au for the source and drain.

3. CONCLUSIONS

This paper simulates the DC characteristics of different structured vertical GaN devices to analyze the main parameters affecting the basic performance of vertical GaN DT-MOS. Based on the simulation results, the vertical p-GaN island double trench MOS is optimized, and it is found that the new designed vertical p-GaN island double trench MOS can achieve a good trade-off between high breakdown voltage and low on-resistance, generating a BFOM of up to 1.34 GW/cm². The p-GaN structure located under the gate can enhance the breakdown voltage while effectively reducing the peak electric field in the gate oxide, further increasing the off-state breakdown voltage to 1744V. In addition, this design significantly reduces the gate leakage current, reducing the HF-FOM of the optimized DT-MOS by 47%, greatly improving the switching loss of the device, showing the potential application of vertical GaN power MOSFET devices in high-frequency switching.

It is proposed for the first time to realize heavily doped P-type shielding structure by P-type GaN selection growth mode and P-type GaN island under gate by ion implantation process. The combination of these two processes can greatly reduce impurity defects introduced by Mg ion implantation and improve device performance. At the same time, it can also be combined with Si-based CMOS process to reduce production cost. Currently, most research on vertical GaN transistors, both domestically and internationally, is focused on theoretical studies and experimental exploration due to challenges related to material costs, quality, and long-term reliability. The novel vertical p-GaN island dual-channel MOSFET presented in this paper has demonstrated, through theoretical analysis, its potential for high-voltage and high-power applications. Consequently, advancing the growth of high-quality GaN single crystals and evaluating the reliability of vertical GaN devices are essential future directions. These efforts will enable vertical devices to fully capitalize on their advantages over horizontal counterparts, thereby expanding the market share and industrial scope of GaN materials and devices in the global semiconductor industry.

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