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Macroporous Silicon Structures for Light Harvesting

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Macroporous silicon light trapping layers on the surface of p-type substrates were manufactured by using electrochemical etching in electrolyte containing organic solvent and under potentiostatic conditions. Equilibrium state where pore size and orientation slightly depend on the etching time was observed under potentiostatic etching conditions. Optical measurements have shown the decreased optical reflection as compared to bulk silicon. The p-n junction was formed by phosphorus diffusion from phosphosilicate glasses. Scanning Kelvin Force Microscopy technique was used to determine the location of p-n junction in samples with porous silicon layers.
Keywords: porous silicon, antireflection coatings, p-n junction.

1. INTRODUCTION

Solar energy is the third most important renewable energy source after hydro and wind power. A capacity of solar energy devices installed over the world is growing from about 10 GW in 2007 to 102 GW in 2012 [1]. Crystal silicon (c-Si) based devices still play a major role in the market with 80 % of share. The main cause of this is the maturity of the technology and cost reducing over time. Considering the solar energy conversion efficiency, c-Si-based devices stand in the third position with 25 % [2] for laboratory-made solar cells. There is a lot of interest to develop low cost technologies for increasing efficiency or reducing cost for manufacturing.

One of the methods to increase the solar cell efficiency is to reduce a reflectivity from the surface and increase absorbance of light with photon energies below the silicon band-gap [3]. The reflectivity usually is reduced by using antireflective coatings (ARC) such as silicon nitride or titanium oxide layers [4]. However, this technique is effective only in a limited spectral range. Another approach is to modify silicon surface topography by micro- or nano-texturing [5]. Micro texturing is a very interesting method because of the light trapping effect inside the hundreds of nanometers or micrometer size pores (macroporous silicon). The surface texturing can be performed by various techniques such as reactive ion etching, nanolithography, chemical, electrochemical etching and metal assisted etching [6]. Electrochemical etching has the main advantage of its low cost and simple instrumentation. It can be used for large area samples as well as for small area samples [7] for System On Chip (SOC). Electrochemical etching is efficient technique for microtexturing of n-type silicon substrates. However, there are problems and limitations when we deal with electrochemical formation of macropores for light trapping layers in the medium doped p-type substrates that are used in manufacturing process [8]. Also, difficulties are met in the formation of the shallow p-n junction.

The aim of this work was to produce by electrochemical etching and investigate the c-Si-based structures with macroporous Si (por-Si) light trapping layers (LTL) on p-type substrates and to form the p-n junction below the por-Si layer.

2. EXPERIMENTAL

In this work por-Si layers were made by using a low cost electrochemical etching technique. This technique is suitable to produce a good quality por-Si layers on silicon substrates and on the surface of integrated SOC solar cells. The (100)-oriented commercially available p-type $0.5\ \Omega\cdot cm - 3\ \Omega\cdot cm$ silicon substrates were cleaned using RCA clean [9]. 70 % HF (Chempur, Poland) and DMF (EKOS-1, Russia) were used as received and mixed in ratio $HF : DMF = 1 : 10$. Electrochemical etching was carried in PTFE cell for 5, 15 or 30 min. at potentiostatic regime at 30 V or 40 V in the dark.

The p-n junction was formed by using phosphorus diffusion from phosphosilicate glasses (PSG). A solution consisting of $TEOS : C_2H_5OH : H_2O : HCl = 5 : 10 : 1 : 0.1$ (kept for 24 h) was mixed with phosphoric acid and deposited on por-Si ARC by spin-coating. The structure was dried for 1 h at 80 ºC in ambient atmosphere and annealed using RTP furnace (UniTemp RTP-1300) for 1 min. at 800 ºC in nitrogen atmosphere. After diffusion process, a residue of the reaction was removed by immersing the samples in dilute HF solution.

Surface morphology of por-Si LTL was examined by scanning electron microscope Hitachi TM-3000. Optical measurements were carried out by using SHIMADZU UV-3600 spectrometer with integrating sphere. The location of p-n junction was detected on freshly cleaved sample by using DM3100/Nanoscope IVa (Veeco Metrology Group, USA) by cross-sectional surface potential measurements. Ohmic contacts for SKFM measurements were made by depositing silver contacts on the back side of the silicon.

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2. RESULTS

Macroporous silicon layer formation on p-type substrates using electrochemical etching is complicated. When the standard water-diluted HF electrolyte is used, a two-layers porous silicon structure is formed with top nanoporous layer consisting of silicon dioxide with silicon nanoparticles and bottom monocrystaline nanoporous layer with pores with diameter of few or tens of nanometers [10]. Top nanoporous layer can be easily removed by KOH solution, but bottom layer is not appropriate to be used as a light-trapping layer because the pore diameter is too small. In order to increase the light scattering within the layer, the size of pores or structures should be comparable with the wavelength of the incident light (400 nm – 1000 nm). To form such structures a different electrolyte is to be used. It was shown that etching in electrolytes with organic solvent may led to macroporous silicon formation on p-type substrates. There are two main differences between aqueous and organic solvent HF-electrolyte: 1) organic solvent is characterized by its own "oxidation power" and influence on oxidation reactions. The resulting products are soluble in electrolyte; 2) etching rate with organic solvent is higher because there are no reaction products with Si-OH bonds whereas the products with Si-F lead to a faster silicon dissolution. Several organic solvents such as acetonitrile (MeCN), propylene carbonate (PC), dimethylformamide (DMF) and dimethylsulfoxide (DMSO) were tested. DMF has a main advantage that etching in electrolyte with DMF leads to the formation of one-layer macroporous silicon structure while the top nanoporous layer is absent [11] and hence the etching rate of the pores is. In our work we used 70 % HF to reduce amount of water electrolyte and to increase the role of DMF. A decision to use the potentiostatic etching regime instead of de facto standart galvanostatic was inspired by the following idea: At constant voltage, a high current at the start of etching occurs resulting in the formation of the pore tip of higher diameter. After some time, the current decreases as the resistivity of the porous layer increases. At the equilibrium etching state, the cone-like pores are formed because the etching rate differs for various crystallographic orientations. For high-resistivity electrolyte with DMF, high voltages must be used in the etching process.

From quantitative analysis of the data presented in SEM micrographs of the top view of the structures (Fig. 1) it follows that the size-distribution of pores and the average pore size do not depend on the etching time (a, b or c, d). However, the pore size decreases from 0.7 μm to 0.5 μm when the etching voltage is increased from 30 V to 40 V (a, c).

From cross-view SEM micrographs (Fig. 2) we can see that cone-like pores are formed (a, b, c) and the depth and size of the pores do not depend on the etching time for the etching voltage 30 V (a, b). However, for the structures etched at 40 V, an increase of etching time influences the shape of pores: the cone-like pores (d) become cylindrical ones that are perpendicular to the surface (c). This change can be explained by the occurrence of anisotropic etching due to passivation of pore walls. We propose that etching p-type substrates in HF electrolyte containing DMF in potentiostatic regime can lead to the equilibrium state

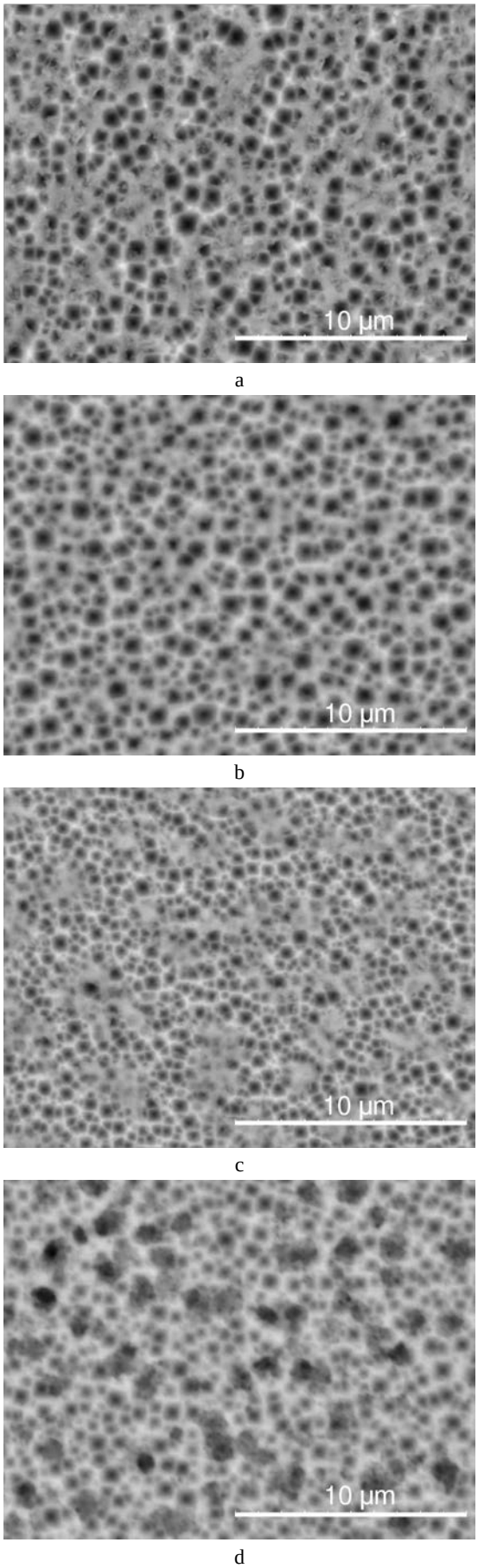
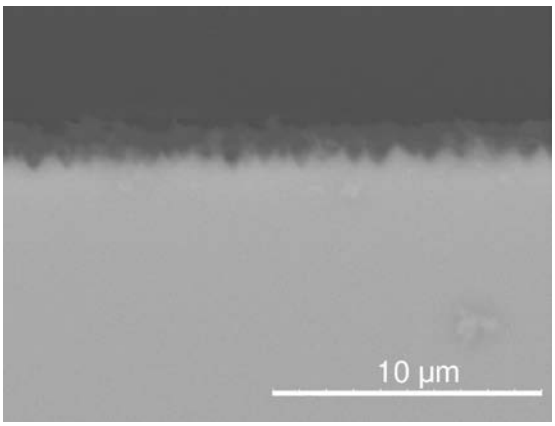
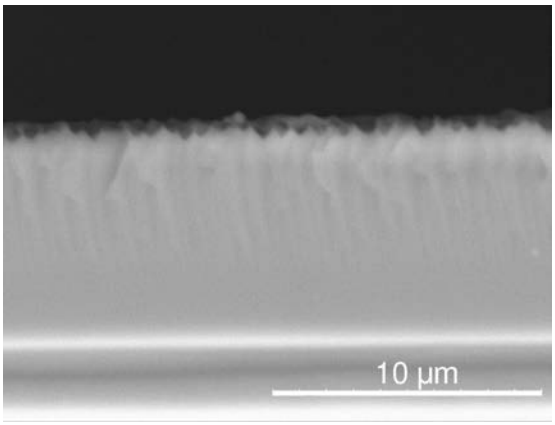


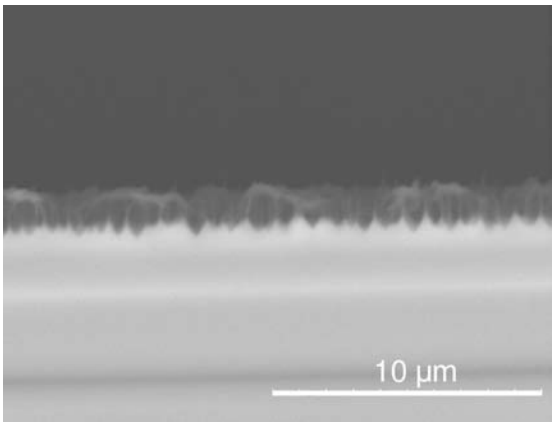
Fig. 1. Top view of por-Si layers produced by etching: a – 30 V, 15 min.; b – 30 V, 30 min.; c – 40 V, 15 min.; d – 40 V, 5 min.



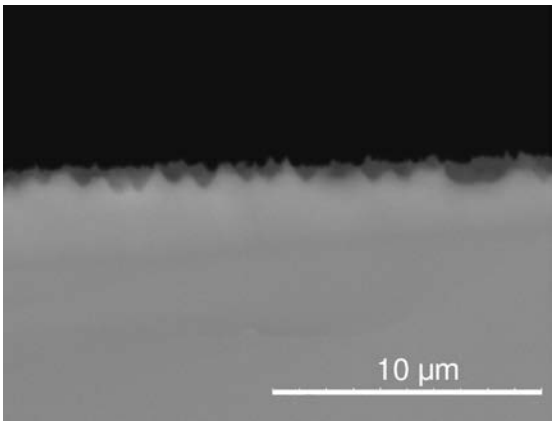
a



b



c



d

Fig. 2. Cross-sectional view of por-Si layers produced by etching: a – 30 V, 15 min.; b – 30 V, 30 min.; c – 40 V, 15 min.; d – 40 V, 5 min.

where pore size and orientation slightly depend on the etching time.

Optical measurements were carried out to reveal the advantages of the formed structures for light harvesting. The measurements have shown (Fig. 3) the reflectance to be by 66 % less than that in bulk silicon. For the light with photon energies below the silicon band gap, the transmittance (Fig. 4) decreased by 82 % as compared to bulk silicon transmittance. These changes lead to the increase of internal quantum efficiency for structures with por-Si layer.

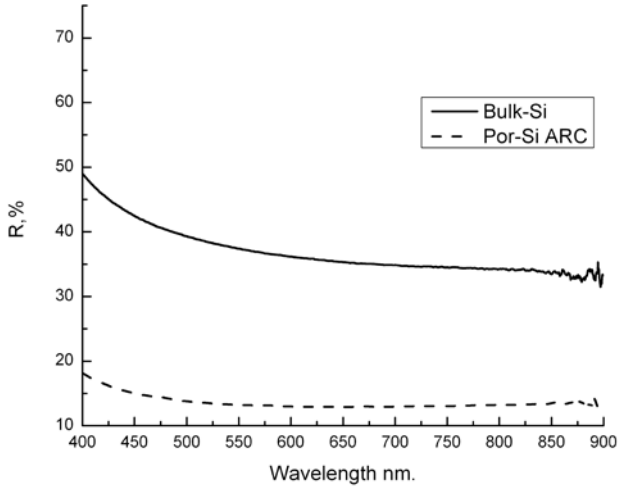


Fig. 3. Normal light incidence reflectance spectra of the structures without (bulk Si) and with por-Si layer formed by electrochemical etching in 40 V for 5 min.

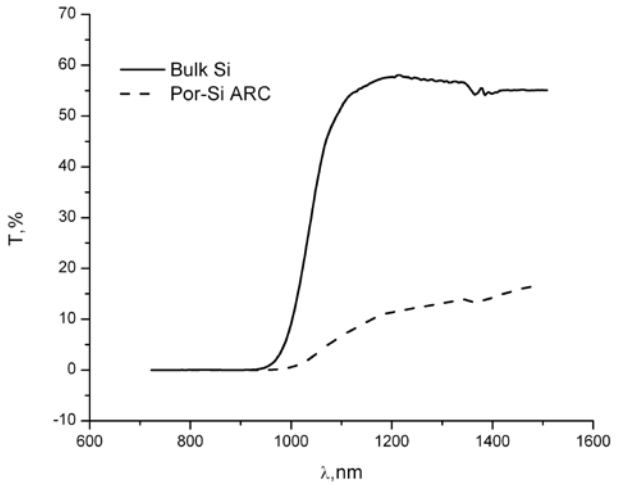


Fig. 4. Transmission spectra of the structures without (bulk Si) and with por-Si layer formed by electrochemical etching in 40 V for 5 min.

Another problem in the application of por-Si layers in light harvesting is the formation of p-n junction. It should be noted that even the indication of the junction depth and its visualisation are rather complicated. For our structures we formed p-n junction from phosphosilicate glasses and used the RTP process to form a shallow junction. For the junction depth measurements and its visualisation we used a well-known Scanning Kelvin Force Microscopy (SKFM) technique. Using the SKFM technique, the surface topography simultaneously with contact potential difference

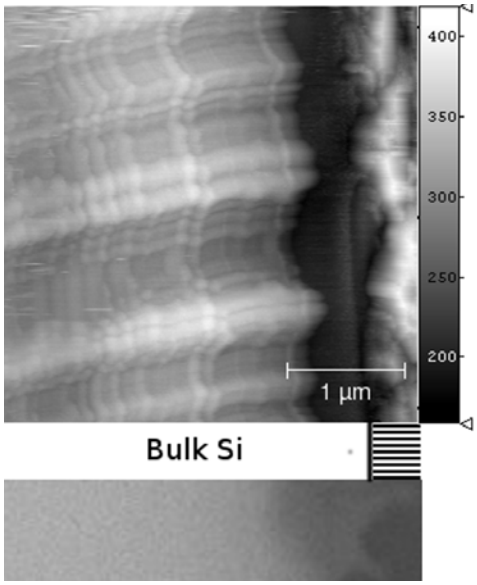


Fig. 5. The p-n junction visualisation using SKFM (scan size: 3.5 um, step length: 13 nm) (top of the picture) and SEM micrograph (bottom of the picture). Grid in the right side shows the location of por-Si layer. Top surface of the sample is in the right side. CPD value scale in mV

(CPD) between the probe and sample surface was measured. As CPD is different for n and p type silicon, the location of p-n junction can be determined. Cross-sectional CPD map in Fig. 5 shows the semi-ring like contrast line between bright and dark areas of p- and n-type materials, that follows the bottom line of por-Si layer. Comparing the edge of the sample surface visualised by SPM and SEM we can suppose that the mean value of the junction location is 500 nm below the porous layer. The bright color in cross-sectional CPD map represents p-type material far (> 500 nm) from the bottom and top of the sample surface, but near the interface pore wall/air surface band bending can disturb CPD signal. The surface band bending effect can explain bright area at the right side (near the edge of the sample) of the top image in Fig. 5.

4. CONCLUSIONS

Macroporous (up to 0.7 µm in diameter) cone-like structures on p-type silicon substrates were made using electrochemical etching technique in electrolyte containing organic solvent and under potentiostatic conditions. Unlike the etching in galvanostatic etching mode an equilibrium state where pore size and orientation slightly depend on the etching time was fixed for the electrochemical etching in potentiostatic mode. Por-Si layers have shown the optical properties suitable for the light harvesting applications. P-n junction was formed and located 500 nm below the porous layer.

Acknowledgments

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